David **Parello**

Associate Professor in Computer Science

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Summary

University of Perpignan Via Domicia — *Perpignan, France*

Associate professor in Computer Science — *current position*

On one hand my research interests concern the performance of many-core micro-architectures and their programming models. Today's many-core designs are based on more than twenty years of single core incremental design implementations. Consequently micro-architecture components are well suited for single thread performance and centralized model of execution but not for parallel executions. We believe that many-core designs need to be revisited to efficiently exploit parallelism.

On the other hand my research focus on numerical accuracy of high performance computing. High performance computing software, such as numerical simulation may suffer from floating-point errors. Such errors affect reproducibility and accuracy. We aim to provide useful libraries to improve both reproducibility and accuracy.

Experience

University of Perpignan Via Domicia — *Perpignan, France*

Associate professor in Computer Science — *2005 - present*

- Member of the DALI team from LIRMM laboratory.

University of Perpignan Via Domicia — *Perpignan, France*

Head of the Mathematics and Computer Science Department — *2012 - 2014*

University of Paris-Sud/Orsay — *Orsay, France*

Temporary Assistant Professor — *2004 - 2005*

University of Paris-Sud/Orsay — *Orsay, France*

Ph.D. Candidate at University of Paris-Sud/Orsay and Hewlett-Packard France (CIFRE) — *2000 - 2004*

- Member of the *ex*-ALCHEMY (Architectures, Languages and Compilers to Harness the End of Moore Years) team at LRI/INRIA.
- Member of pre-sales team at HP France.

Education

University of Paris-Sud/Orsay — *Orsay, France*

Ph.D. in Computer Science at University of Paris-Sud/Orsay — *2000 - 2005*

- Title: Program optimization methodology for complex processor architectures.
- Advisors: Olivier Temam and Jean-Marie Verdun.

University of Paul Sabatier, Toulouse III — *Toulouse, France*

Master of Science (M.S.) in Computer Science — *1998 - 2000*

University of Paul Sabatier, Toulouse III — *Toulouse, France*

Bachelor of Science (B.S.) in Computer Science — *1994 - 1998*

Former Ph.D.

University of Perpignan *Perpignan, France*

Ph.D. former *2006 - 2017*

- Chemseddine Chohra, "Toward Reproducible, accurately rounded and efficient BLAS" (2017)
- Ke Chen, "Improving processor performance throught dynamic extraction of instruction level parallelism" (2012)
- Ali El Moussaoui, "A step toward ILP processor" (2011)
- Mourad Bouache, "Tools for analysis and evaluation of a CPU performance" (2008)

Publications

Articles in International Journals

Articles in International Conferences

Articles in National Journals and Conferences