Groupe de travail – Équipe ARITH, LIRMM

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Implementation of binary floating-point arithmetic on embedded integer processors

Polynomial evaluation-based algorithms and certified code generation

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Arénaire INRIA project-team (LIP, Ens Lyon)   Université de Lyon   CNRS

Motivation

- Embedded systems are ubiquitous
  - microprocessors dedicated to one or a few specific tasks
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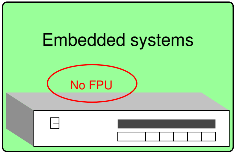

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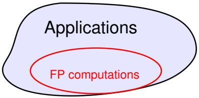

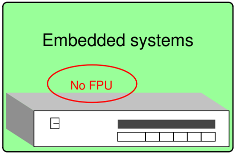

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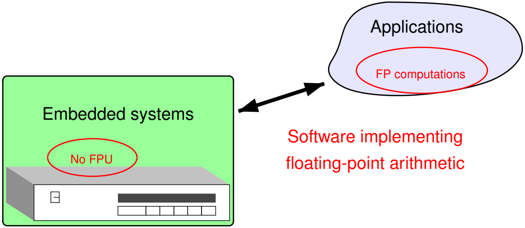

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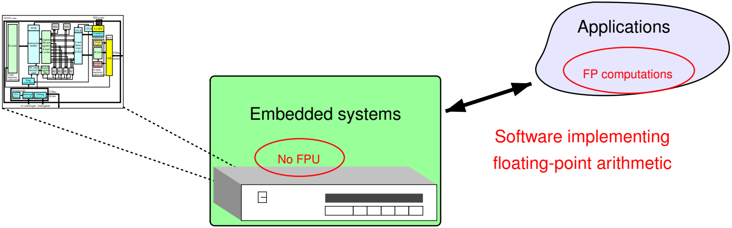

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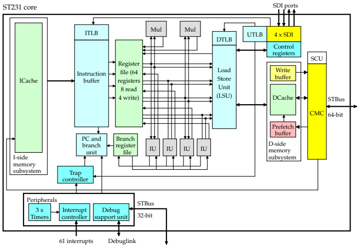
Overview of the ST231 architecture



- 4-issue VLIW 32-bit integer processor
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- Parallel execution unit
  - 4 integer ALU
  - 2 pipelined multipliers $32 \times 32 \rightarrow 32$
- Latencies: ALU $\rightarrow$ 1 cycle, Mul $\rightarrow$ 3 cycles

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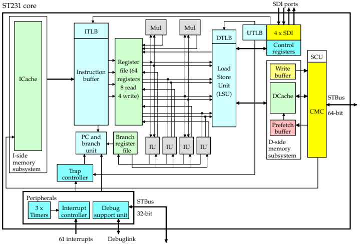

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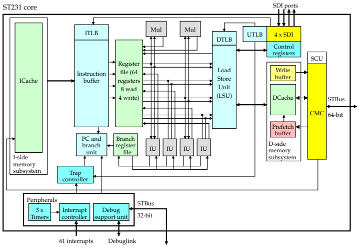

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```
uint32_t R1 = A0 + C;
uint32_t R2 = A3 * X;
uint32_t R3 = A1 * X;
uint32_t R4 = X * X;
```

	Issue 1	Issue 2	Issue 3	Issue 4
0	R1	R2		R3
1	R4			

How to emulate floating-point arithmetic in software?

Design and implementation of efficient software support for IEEE 754 floating-point arithmetic on integer processors

- Existing software for IEEE 754 floating-point arithmetic:
  - Software floating-point support of GCC, Glibc and μClibc, GoFast Floating-Point Library
  - SoftFloat ($\longrightarrow$ STlib)
  - FLIP (Floating-point Library for Integer Processors)
    - software support for *binary32* floating-point arithmetic on integer processors
    - correctly-rounded addition, subtraction, multiplication, division, square root, reciprocal, ...
    - handling subnormals, and handling special inputs

Towards the generation of fast and certified codes

- Underlying problem: development "by hand"
  - long and tedious, error prone
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- Current challenge: tools and methodologies for the automatic generation of efficient and certified programs
  - optimized for a given format, for the target architecture

Towards the generation of fast and certified codes

- Arénaire's developments: hardware (FloPoCo) and software (Sollya, Metalibm)

- Spiral project: hardware and software code generation for DSP algorithms

  Can we teach computers to write fast libraries?

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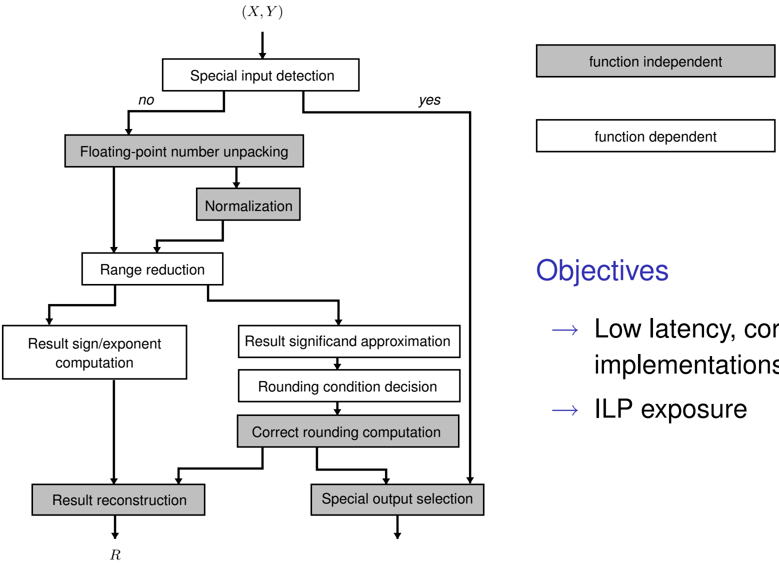
  Can we teach computers to write fast libraries?

- Our tool: CGPE (Code Generation for Polynomial Evaluation)

  In the particular case of ***polynomial evaluation****, can we teach computers to write* ***fast and certified*** *codes, for a given target and optimized for a given format?*

Basic blocks for implementing correctly-rounded operators



Objectives

$\longrightarrow$ Low latency, correctly-rounded implementations

$\longrightarrow$ ILP exposure

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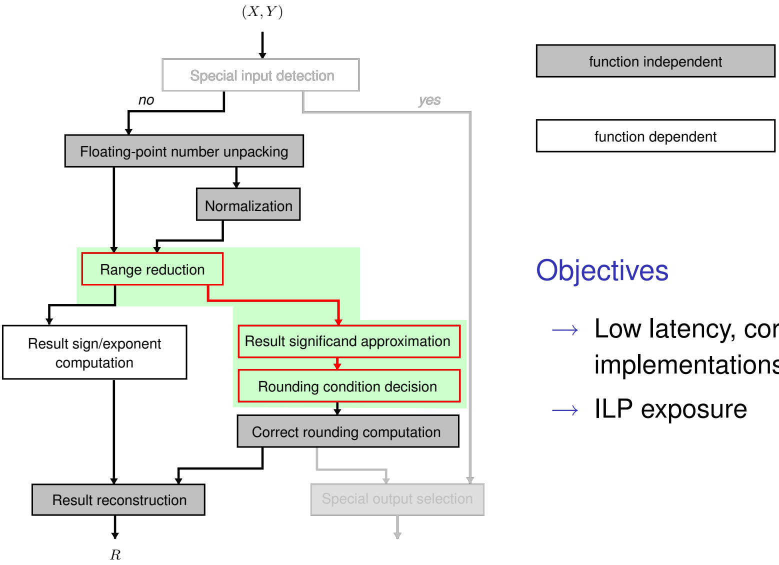

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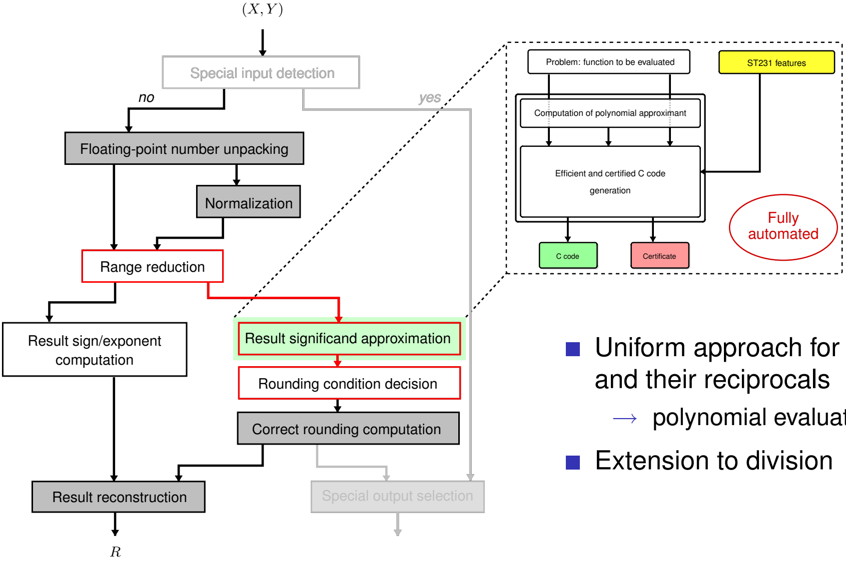
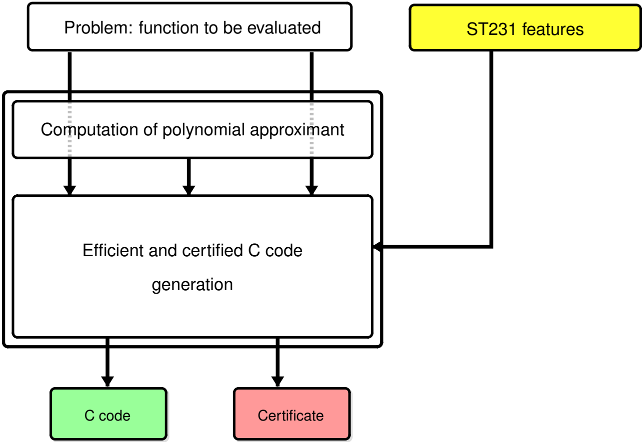


- Uniform approach for *n*th roots and their reciprocals
  - $\longrightarrow$ polynomial evaluation
- Extension to division

Flowchart for generating efficient and certified C codes



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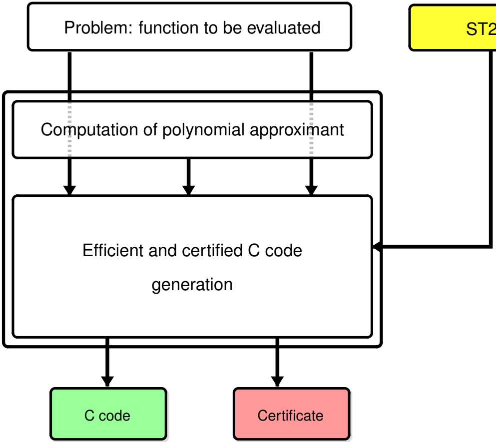

Constraints

- Accuracy of approximant and C code

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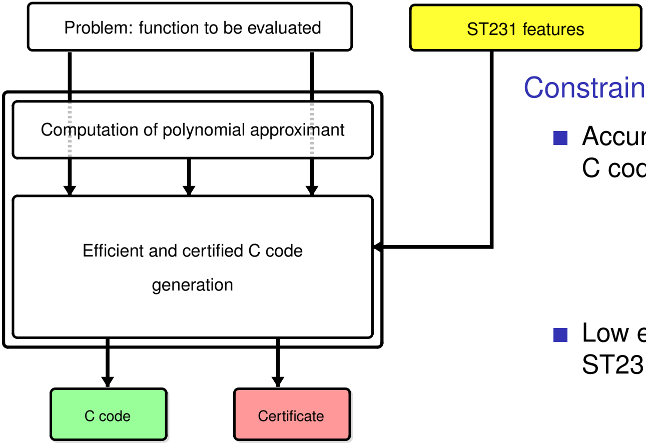

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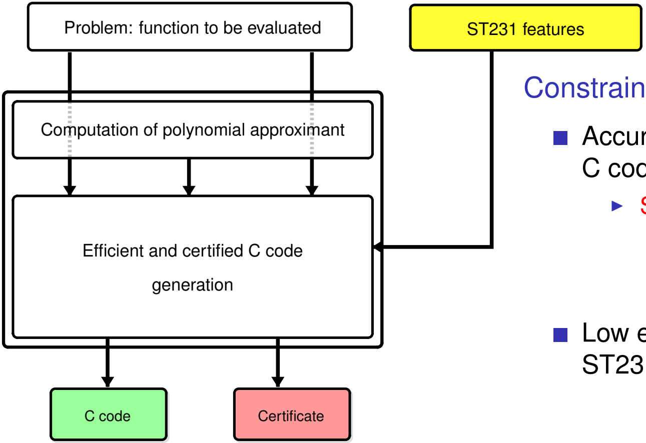

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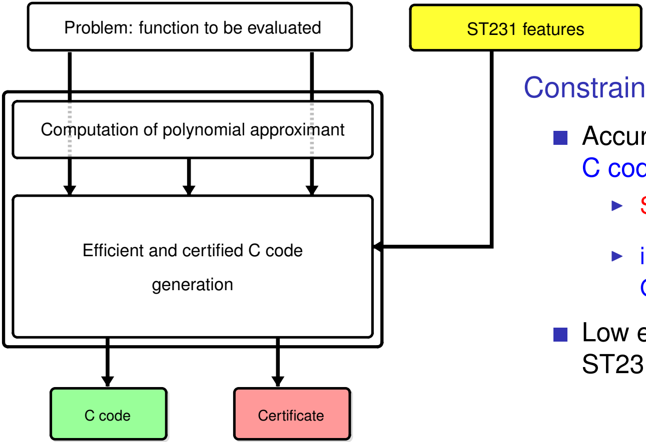

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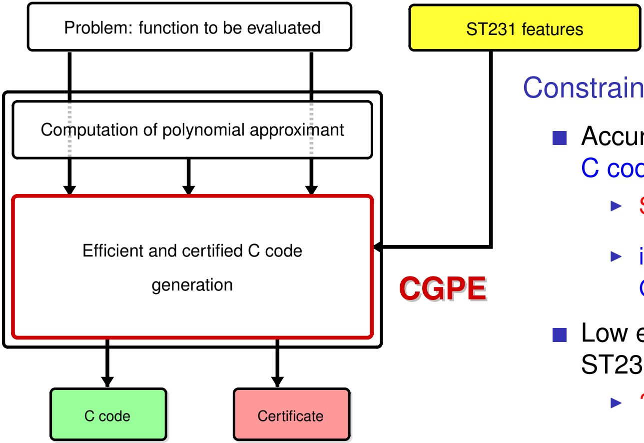

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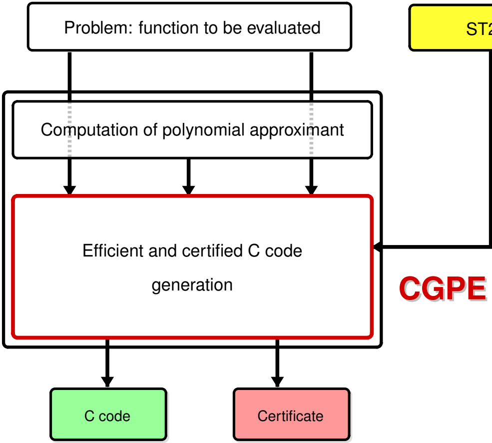

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- Efficiency of the generation process

Outline of the talk

1. Design and implementation of floating-point operators
   - Bivariate polynomial evaluation-based approach
   - Implementation of correct rounding
2. Low latency parenthesization computation
   - Classical evaluation methods
   - Computation of all parenthesizations
   - Towards low evaluation latency
3. Selection of effective evaluation parenthesizations
   - General framework
   - Automatic certification of generated C codes
4. Numerical results
5. Conclusions and perspectives

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Notation and assumptions

$$(x, y) \longrightarrow \boxed{\text{Division C code}} \longrightarrow \mathrm{RN}(x/y)$$

- Input (x, y) and output $\mathrm{RN}(x/y)$: normal numbers
  - $\longrightarrow$ no underflow nor overflow
  - $\longrightarrow$ precision p, extremal exponents $e_{\min}$, $e_{\max}$

$$x = \pm 1.m_{x,1} \ldots m_{x,p-1} \cdot 2^{e_x} \quad \text{with} \quad e_x \in \{e_{\min}, \ldots, e_{\max}\}$$

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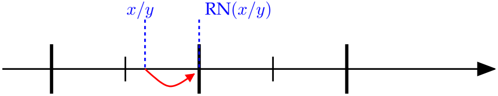
  - → RoundTiesToEven



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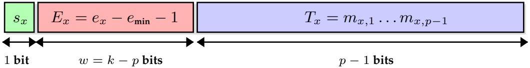
- Standard binary encoding: k-bit unsigned integer X encodes input x



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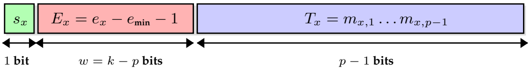

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Range reduction of division

- Express the exact result $r = x/y$ as:

$$r = \ell \cdot 2^d \quad \Rightarrow \quad \mathrm{RN}(x/y) = \mathrm{RN}(\ell) \cdot 2^d$$

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$$\ell \in [1,2) \quad \text{and} \quad d \in \{e_{\min}, \ldots, e_{\max}\}$$

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How to compute the correctly-rounded significand $\mathrm{RN}(\ell)$?

Methods for computing the correctly-rounded significand

- Iterative methods: restoring, non-restoring, SRT, ...
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- Polynomial-based methods
  - Agarwal, Gustavson and Schmookler (1999)
    $\longrightarrow$ univariate polynomial evaluation
  - Our approach
    $\longrightarrow$ bivariate polynomial evaluation: maximal ILP exposure

Correct rounding via truncated one-sided approximation

- How to compute RN(ℓ), with $\ell = 2^{1-c} \cdot m_x / m_y$?

- Three steps for correct rounding computation

  1. compute $v = 1.v_1 \ldots v_{k-2}$ such that $-2^{-p} \leq \ell - v < 0$
     - $\rightarrow$ implied by $|(\ell + 2^{-p-1}) - v| < 2^{-p-1}$
     - $\rightarrow$ bivariate polynomial evaluation
  2. compute u as the truncation of v after p fraction bits
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How to compute the one-sided approximation v and then deduce $\mathrm{RN}(\ell)$?

One-sided approximation via bivariate polynomials

1. Consider $\ell + 2^{-p-1}$ as the exact result of the function

$$F(s,t) = s/(1+t) + 2^{-p-1}$$

at the points $s^* = 2^{1-c} \cdot m_x$ and $t^* = m_y - 1$

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2. Approximate $F(s,t)$ by a bivariate polynomial $P(s,t)$

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$\longrightarrow$ $a(t)$: univariate polynomial approximant of $1/(1+t)$

$\longrightarrow$ approximation error E_{approx}

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$$v = \mathcal{P}(s^*, t^*)$$

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How to ensure that $|(\ell + 2^{-p-1}) - v| < 2^{-p-1}$?

Sufficient error bounds

- To ensure $\quad |(\ell + 2^{-p-1}) - v| < 2^{-p-1}$

  it suffices to ensure that $\quad \mu \cdot E_{\text{approx}} + E_{\text{eval}} < 2^{-p-1}$,

  since

$$|(\ell + 2^{-p-1}) - v| \leq \mu \cdot E_{\text{approx}} + E_{\text{eval}} \qquad \text{with} \qquad \mu = 4 - 2^{3-p}$$

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$$E_{\mathrm{approx}} \le \theta \quad \text{with} \quad \theta < 2^{-p-1}/\mu \qquad \Rightarrow \qquad E_{\mathrm{eval}} < \eta = 2^{-p-1} - \mu \cdot \theta$$

Example for the *binary32* division

- Sufficient conditions with $\mu = 4 - 2^{-21}$

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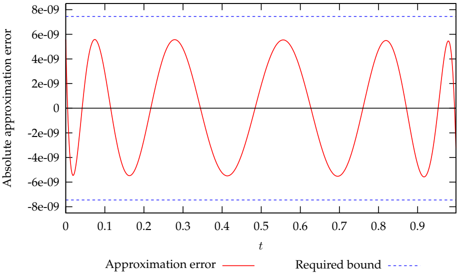
- Approximation of $1/(1+t)$ by a Remez-like polynomial of degree 10



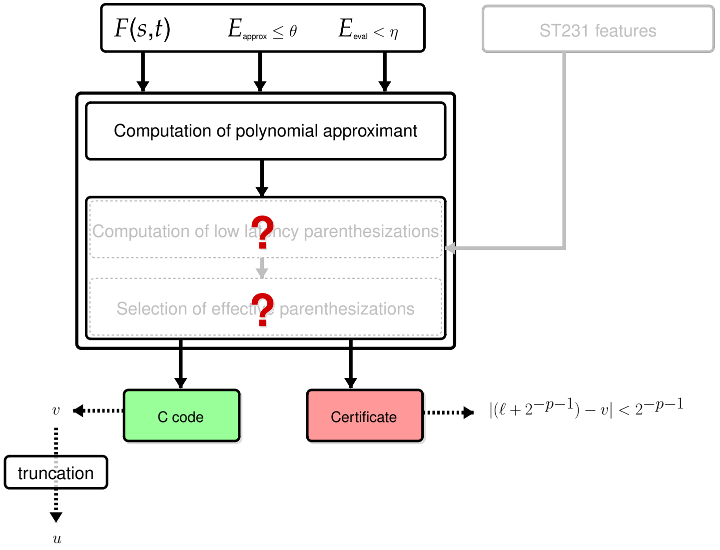
- $E_{\text{approx}} \leq \theta$,

  with $\theta = 3 \cdot 2^{-29} \approx 6 \cdot 10^{-9}$

- $E_{\text{eval}} < \eta$,

  with $\eta \approx 7.4 \cdot 10^{-9}$

Flowchart for generating efficient and certified C codes

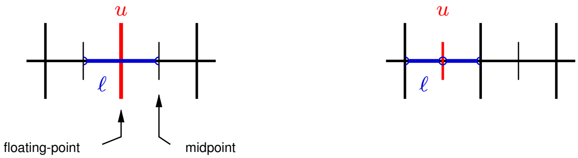


Rounding condition: definition

- Approximation u of ℓ with

$$\ell = 2^{1-c} \cdot m_x / m_y$$

- The exact value ℓ may have an infinite number of bits
  - $\longrightarrow$ the sticky bit cannot always be computed



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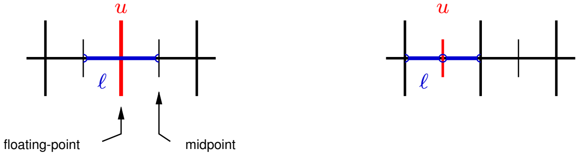


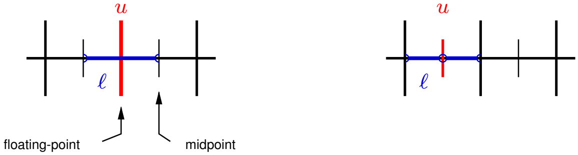
- Compute RN(ℓ) requires to be able to decide whether $u \geq \ell$
  - $\longrightarrow$ ℓ cannot be a midpoint

Rounding condition: definition

- Approximation u of ℓ with

$$\ell = 2^{1-c} \cdot m_x / m_y$$

- The exact value ℓ may have an infinite number of bits
  - $\longrightarrow$ the sticky bit cannot always be computed

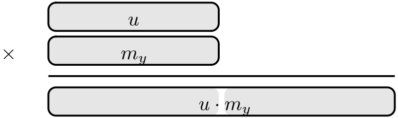


- Compute RN(ℓ) requires to be able to decide whether $u \geq \ell$
  - $\longrightarrow$ ℓ cannot be a midpoint
- Rounding condition: $u \geq \ell$

$$u \geq \ell \quad \Longleftrightarrow \quad u \cdot m_y \geq 2^{1-c} \cdot m_x$$

Rounding condition: implementation in integer arithmetic

- Rounding condition: $u \cdot m_y \geq 2^{1-c} \cdot m_x$
- Approximation u and m_y: representable with 32 bits



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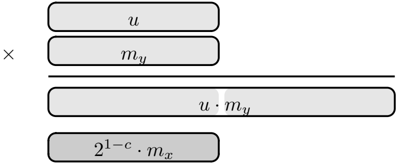

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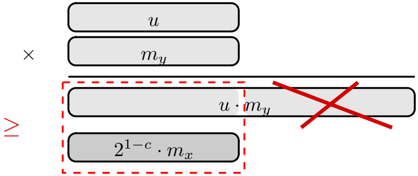

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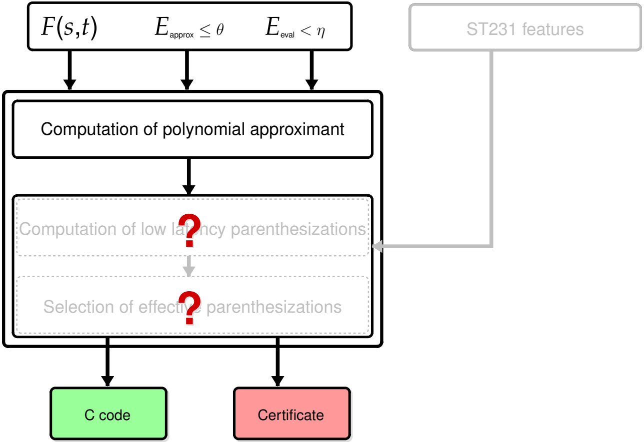
$\Rightarrow$ one $32 \times 32 \rightarrow 32$-bit multiplication and one comparison

Flowchart for generating efficient and certified C codes



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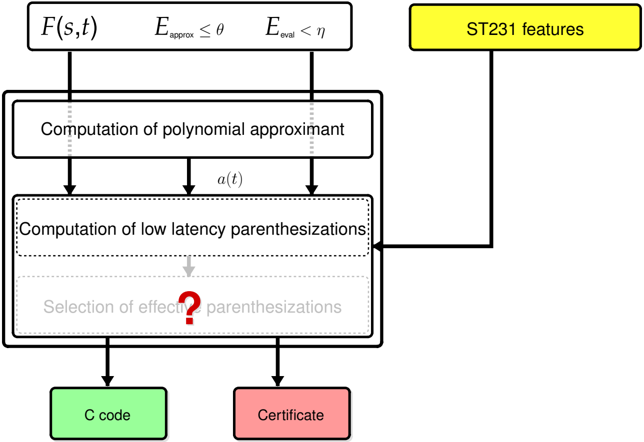

Outline of the talk

1. Design and implementation of floating-point operators

2. Low latency parenthesization computation
   - Classical evaluation methods
   - Computation of all parenthesizations
   - Towards low evaluation latency

3. Selection of effective evaluation parenthesizations

4. Numerical results

5. Conclusions and perspectives

Objectives

- Compute an efficient parenthesization for evaluating $P(s,t)$
  - $\longrightarrow$ reduces the evaluation latency on unbounded parallelism

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Classical parenthesizations for *binary32* division

$$P(s,t) = 2^{-25} + s \cdot \sum_{0 \le i \le 10} a_i t^i$$

- Horner's rule: $(3+1) \times 11 = 44$ cycles
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- ...

We can do better.

How to explore the solution space of parenthesizations?

Algorithm for computing all parenthesizations

$$a(x,y) = \sum_{0 \le i \le dx} \sum_{0 \le j \le n_y} a_{i,j} \cdot x^i \cdot y^j \quad \text{with} \quad n = n_x + n_y, \quad \text{and} \quad a_{n_x,n_y} \neq 0$$

Example

Let $a(x,y) = a_{0,0} + a_{1,0} \cdot x + a_{0,1} \cdot y + a_{1,1} \cdot x \cdot y$. Then

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- Exhaustive algorithm: iterative process
  - $\longrightarrow$ step k = computation of all the valid expressions of total degree k
- 3 building rules for computing all parenthesizations

Rules for building *valid* expressions

Consider step k of the algorithm

- $\mathrm{E}^{(k)}$: valid expressions of total degree k
- $\mathrm{P}^{(k)}$: powers $x^i y^j$ of total degree $k = i + j$

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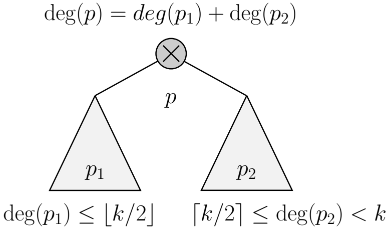
Rule R1 for building the powers



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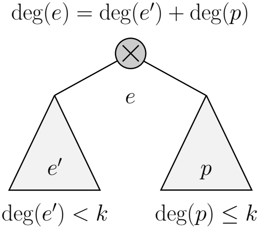
Rule R2 for expressions by multiplications



Rules for building *valid* expressions

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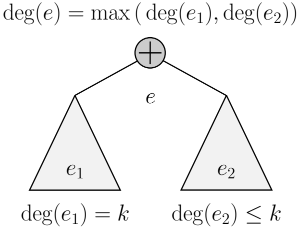
Rule R3 for expressions by additions



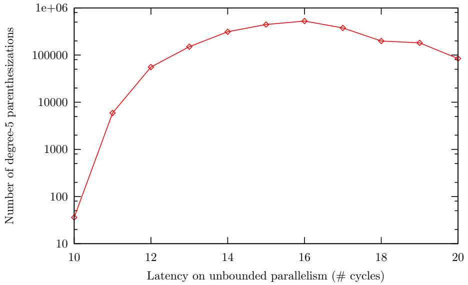
Number of parenthesizations

	$n_x = 1$	$n_x = 2$	$n_x = 3$	$n_x = 4$	$n_x = 5$	$n_x = 6$
$n_y = 0$	1	7	163	11602	2334244	1304066578
$n_y = 1$	51	67467	1133220387	207905478247998	...	...
$n_y = 2$	67467	106191222651	10139277122276921118	...	...	...

Number of generated parenthesizations for evaluating a bivariate polynomial

- Timings for parenthesization computation
  - $\longrightarrow$ for univariate polynomial of degree 5 $\approx$ 1h on a 2.4 GHz core
  - $\longrightarrow$ for bivariate polynomial of degree (2,1) $\approx$ 30s
  - $\longrightarrow$ for $P(s,t)$ of degree (3,1) $\approx$ 7s (88384 schemes)
- Optimization for univariate polynomial and $P(s,t)$
  - $\longrightarrow$ univariate polynomial of degree 5 $\approx$ 4min
  - $\longrightarrow$ for $P(s,t)$ of degree (3,1) $\approx$ 2s (88384 schemes)

Number of parenthesizations



→ minimal latency for univariate polynomial of degree 5: 10 cycles (36 schemes)

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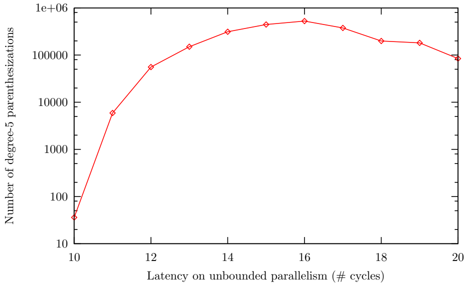

$\longrightarrow$ minimal latency for univariate polynomial of degree 5: 10 cycles (36 schemes)

How to compute only parenthesizations of low latency?

Determination of a *target* latency

- Target latency = minimal cost for evaluating

$$a_{0,0} + a_{n_x,n_y} \cdot x^{n_x} y^{n_y}$$

  - if no scheme satisfies τ then increase τ and restart

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- Static target latency τ_{static}
  - as general as evaluating $a_{0,0} + x^{n_x+n_y+1}$

$$\tau_{\text{static}} = A + M \times \lceil \log_2(n_x + n_y + 1) \rceil$$

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- Dynamic target latency τ_{dynamic}
  - cost of operator on a_{n_x,n_y} and delay on intederminates
  - dynamic programming

Determination of a *target* latency

- Target latency = minimal cost for evaluating

$$a_{0,0} + a_{n_x,n_y} \cdot x^{n_x} y^{n_y}$$

  - if no scheme satisfies τ then increase τ and restart

Example

- Degree-9 bivariate polynomial: $n_x = 8$ and $n_y = 1$
- Latencies: $A = 1$ and $M = 3$
- Delay: y available 9 cycles later than x

τ_{static}	τ_{dynamic}
$1 + 3 \times \lceil \log_2(10) \rceil$ = 13 cycles	16 cycles

Optimized search of *best* parenthesizations

Example

Let $a(x,y)$ be a degree-2 bivariate polynomial

$$a(x,y) = a_{0,0} + a_{1,0} \cdot x + a_{0,1} \cdot y + a_{1,1} \cdot x \cdot y.$$

$\Rightarrow$ find a best splitting of the polynomial $\longrightarrow$ low latency

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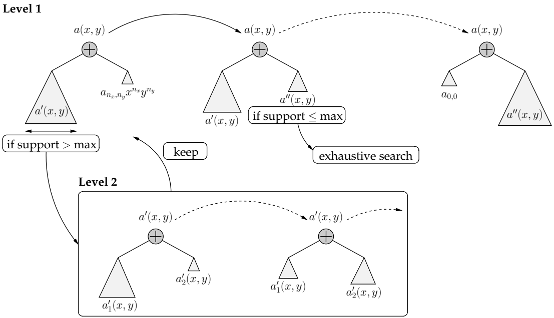


Efficient evaluation parenthesization generation

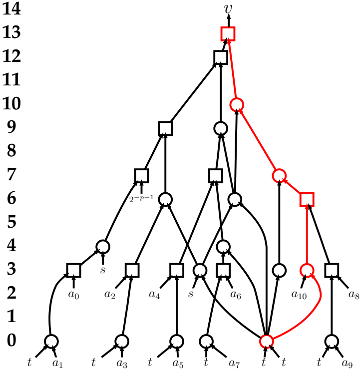
$$P(s,t) = 2^{-25} + s \cdot \sum_{0 \le i \le 10} a_i t^i$$

- First target latency $\tau = 13$
  $\longrightarrow$ no parenthesization found

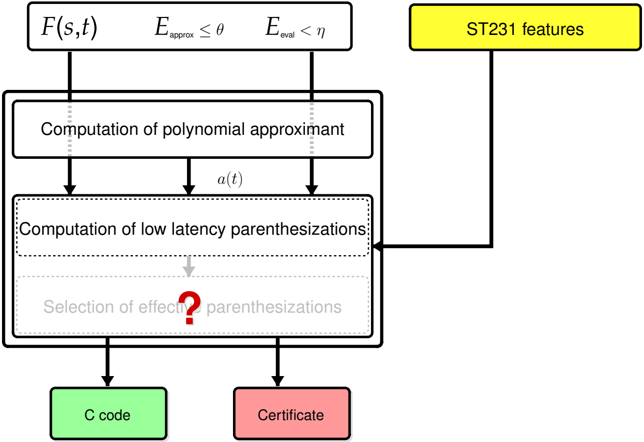
Efficient evaluation parenthesization generation

$$P(s,t) = 2^{-25} + s \cdot \sum_{0 \le i \le 10} a_i t^i$$

- First target latency $\tau = 13$
  - $\longrightarrow$ no parenthesization found
- Second target latency $\tau = 14$
  - $\longrightarrow$ obtained in about 10 sec.
- Classical methods
  - Horner: 44 cycles,
  - Estrin: 19 cycles,
  - Estrin by distributing s: 16 cycles



Flowchart for generating efficient and certified C codes



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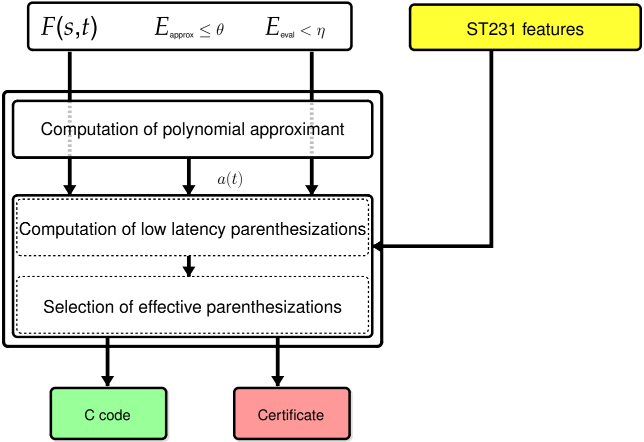

Outline of the talk

1. Design and implementation of floating-point operators
2. Low latency parenthesization computation
3. Selection of effective evaluation parenthesizations
   - General framework
   - Automatic certification of generated C codes
4. Numerical results
5. Conclusions and perspectives

Selection of effective parenthesizations

1. Arithmetic Operator Choice
   - all intermediate variables are of constant sign

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2. Scheduling on a simplified model of the ST231
   - constraints of architecture: cost of operators, instructions bundling, ...
   - delays on indeterminates

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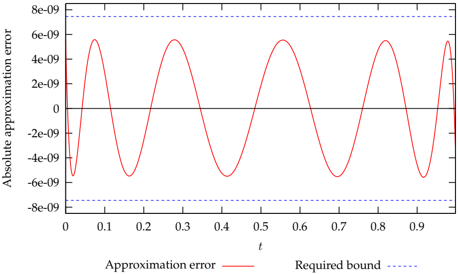
   - all intermediate variables are of constant sign
2. Scheduling on a simplified model of the ST231
   - constraints of architecture: cost of operators, instructions bundling, ...
   - delays on indeterminates
3. Certification of generated C code
   - straightline polynomial evaluation program
   - “certified C code”: we can bound the evaluation error in integer arithmetic

Certification of evaluation error for *binary32* division

- Sufficient conditions with $\mu = 4 - 2^{-21}$

$$E_{\text{approx}} \leq \theta \quad \text{with} \quad \theta < 2^{-25}/\mu \qquad \text{and} \qquad E_{\text{eval}} < \eta = 2^{-25} - \mu \cdot \theta$$



- $E_{\text{approx}} \leq \theta$,

  with $\theta = 3 \cdot 2^{-29} \approx 6 \cdot 10^{-9}$

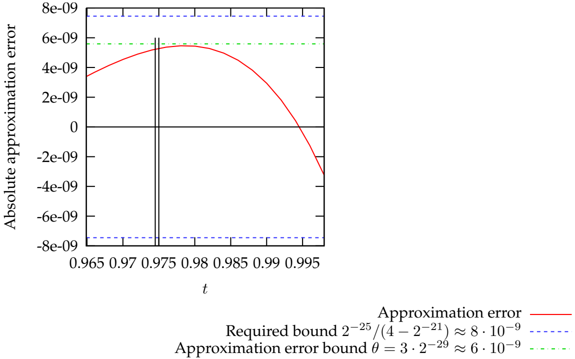
- $E_{\text{eval}} < \eta$,

  with $\eta \approx 7.4 \cdot 10^{-9}$

Certification of evaluation error for *binary32* division

- Case 1: $m_x \geq m_y \rightarrow$ condition satisfied
- Case 2: $m_x < m_y \rightarrow$ condition not satisfied: $E_{\text{eval}} \geq \eta$

$$s^* = 3.935581684112548828125 \text{ and } t^* = 0.974904417991638183593 75$$



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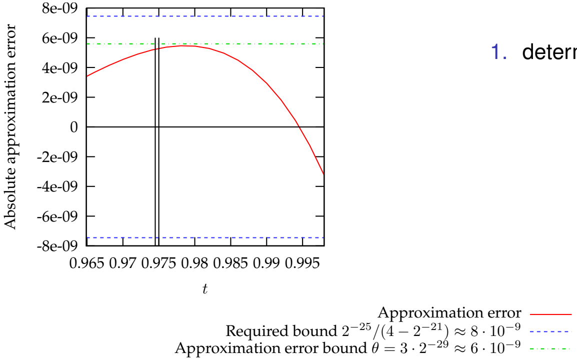

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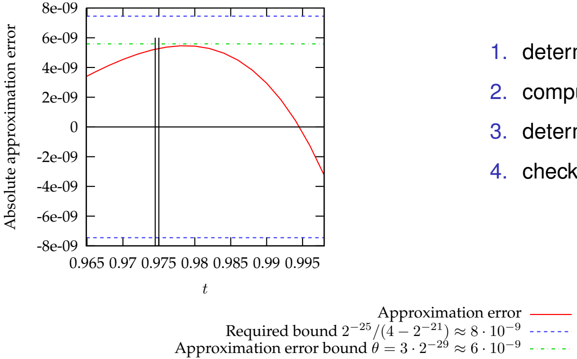
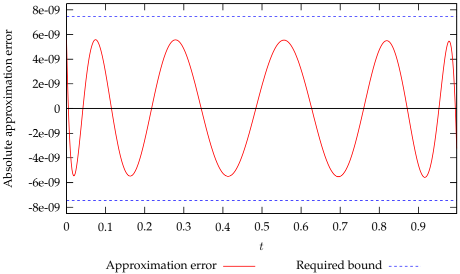


1. determine an interval I around this point
2. compute E_{approx} over I
3. determine an evaluation error bound η
4. check if $E_{\text{eval}} < \eta$?

Certification of evaluation error for *binary32* division

- Sufficient conditions for each subinterval, with $\mu = 4 - 2^{-21}$

$$E_{\text{approx}}^{(i)} \leq \theta^{(i)} \quad \text{with} \quad \theta^{(i)} < 2^{-25}/\mu \qquad \text{and} \qquad E_{\text{eval}}^{(i)} < \eta^{(i)} = 2^{-25} - \mu \cdot \theta^{(i)}$$



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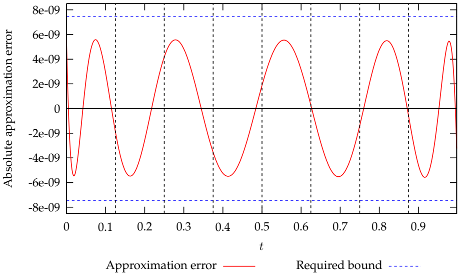

- $E_{\text{approx}}^{(i)} \le \theta^{(i)}$
- $E_{\text{eval}}^{(i)} < \eta^{(i)}$

Certification using a dichotomy-based strategy

- Implementation of the splitting by dichotomy
  - for each $\mathcal{T}^{(i)}$
    1. compute a certified approximation error bound $\theta^{(i)}$
    2. determine an evaluation error bound $\eta^{(i)}$
    3. check this bound: $E_{\text{eval}}^{(i)} < \eta^{(i)}$

  $\Rightarrow$ if this bound is not satisfied, $\mathcal{T}^{(i)}$ is split up into 2 subintervals

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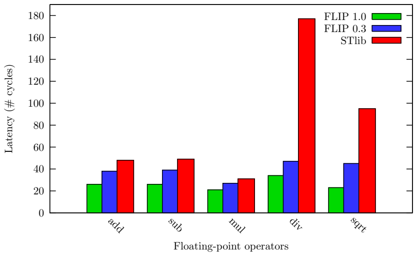
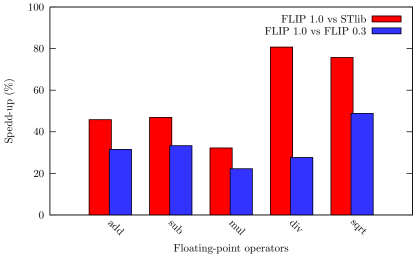
- Example of *binary32* implementation
  - $\longrightarrow$ launched on a 64 processor grid
  - $\longrightarrow$ 36127 subintervals found in several hours ($\approx$ 5h.)

Outline of the talk

Performances of FLIP on ST231





Performances on ST231, in RoundTiesToEven

$\Rightarrow$ Speed-up between 20 and 50 %

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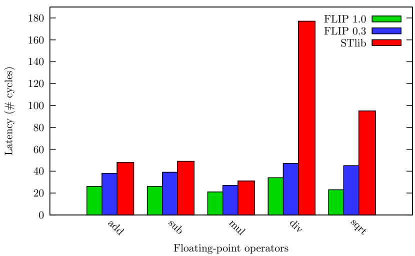

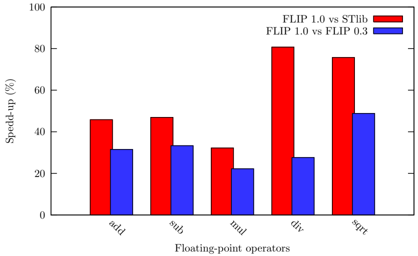

Performances on ST231, in RoundTiesToEven

$\Rightarrow$ Speed-up between 20 and 50 %

- Implementations of other operators

x^{-1}	$x^{-1/2}$	$x^{1/3}$	$x^{-1/3}$	$x^{-1/4}$
25	29	34	40	42

Performances on ST231, in RoundTiesToEven (in number of cycles)

Impact of dynamic target latency

	$x^{1/3}$	$x^{-1/3}$
Degree (n_x, n_y)	(8,1)	(9,1)
Delay on the operand s (# cycles)	9	9
Static *target* latency	13	13
Dynamic *target* latency	16	16
Latency on unbounded parallelism and on ST231	16	16

Latency (# cycles) on unbounded parallelism and on ST231

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$\Longrightarrow$ Conclude on the optimality in terms of polynomial evaluation latency

Timings for code generation

	$x^{1/2}$	$x^{-1/2}$	$x^{1/3}$	$x^{-1/3}$	x^{-1}
Degree (n_x,n_y)	(8,1)	(9,1)	(8,1)	(9,1)	(10,0)
Static target latency	13	13	13	13	13
Dynamic target latency	13	13	16	16	13
Latency on unbounded parallelism	13	13	16	16	13
Latency on ST231	13	14	16	16	13
Parenthesization generation	172ms	152ms	53s	56s	168ms
Arithmetic Operator Choice	6ms	6ms	7ms	11ms	4ms
Scheduling	29s	4m21s	32ms	132ms	7s
Certification (Gappa)	6s	4s	1m38s	1m07s	11s
Total time ($\approx$)	35s	4m25s	2m31s	2m03s	18s

Timing of each step of the generation flow

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Timing of each step of the generation flow

- Impact of the target latency on the first step of the generation
- What may dominate the cost
  - $\longrightarrow$ scheduling algorithm
  - $\longrightarrow$ certification using Gappa

Outline of the talk

1. Design and implementation of floating-point operators
2. Low latency parenthesization computation
3. Selection of effective evaluation parenthesizations
4. Numerical results
5. Conclusions and perspectives

Conclusions

- Design and implementation of floating-point operators
  - uniform approach for correctly-rounded roots and their reciprocals
  - extension to correctly-rounded division

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- Code generation for efficient and certified polynomial evaluation
  - methodologies and tools for automating polynomial evaluation implementation
  - heuristics and techniques for generating quickly efficient and certified C codes

  $\Rightarrow$ CGPE: allows to write and certify automatically $\approx$ 50 % of the codes of FLIP

Perspectives

- Faithful implementation of floating-point operators
  - $\longrightarrow$ other floating-point operators:
    - $\log_2(1+x)$ over $[0.5, 1)$, $1/\sqrt{1+x^2}$ over $[0, 0.5)$, ...
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  - $\longrightarrow$ square root in *binary64*: 171 cycles on ST231, 396 cycles with STlib

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  - $\longrightarrow$ other floating-point operators:
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  - $\longrightarrow$ roots and their reciprocals: rounding condition decision not automated yet
- Extension to other binary floating-point formats
  - $\longrightarrow$ square root in *binary64*: 171 cycles on ST231, 396 cycles with STlib
- Extension to other architectures, typically FPGAs
  - $\longrightarrow$ polynomial evaluation-based approach: already seems to be a good alternative to multiplicative methods on FPGAs
  - $\longrightarrow$ the other techniques introduced of this thesis: should be investigated further

Groupe de travail – Équipe ARITH, LIRMM

Montpellier, France, December 3rd, 2009

Implementation of binary floating-point arithmetic on embedded integer processors

Polynomial evaluation-based algorithms and certified code generation

Guillaume Revy

Advisors: Claude-Pierre Jeannerod and Gilles Villard

Arénaire INRIA project-team (LIP, Ens Lyon) Université de Lyon CNRS